Duration: 3 hours **Max. Marks: 80**

1. **Question No.1 is compulsory.**
2. **Attempt any three from the rest.**
3. **Figure to the right indicates full marks.**
4. **Assume suitable data if it is necessary.**

Q1) Answer any four of the following (entire syllabus)

a. Compare TTL and CMOS logic families. (05)
b. Convert Y= (A+B)(A+C)(B+C) equation into POS form (05)
c. Explain T & D Flip flop (05)
d. Quantization and encoding (05)
e. Compare RAM and ROM memory (05)
f. Compare PLA and PAL (05)

Q2)

a. Convert the given decimal numbers to binary (10)
   i. 25.5
   ii. 10.625
   iii. 0.6875
b. Minimize the four variable function using K-Map (10)
   $f(A,B,C,D) = \Sigma m(0,1,2,3,5,7,8,9,11,14)$

Q3)

a. Explain NAND and NOR as universal gates. (10)
b. Design a full adder circuit by using K-Map. (10)

Q4)

a. Design Binary to Gray code converter. (10)
b. Design and explain MOD - 5 counter. (10)

Q5)

a. Explain R-2R ladder digital to analog convertor. (10)
b. Explain timing diagrams of read and write cycle in case of RAM. (10)

Q6)

a. Draw block diagram of CPLD and explain in detail. (10)
b. Write short note on: (10)
   i. Master slave JK flip flop.
   ii. Content addressable memory.

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